Release Notes for the QNX Neutrino 6.5.0 X86 Update patch#

System requirements#

Target system#

- QNX Neutrino RTOS 6.5.0
- Board version: The following software patch has been verified on the following platforms:
  - Advantech AIMB-580 (Supports Intel® Core™ i7/i5/i3/Pentium® processor with Q57 chipset)
  - Advantech AIMB-270 (Supports Intel® Core™ i7 and i5 mobile processor with Intel QM57 chipset)
  - Advantech PCM-9562 (Embedded Intel® Atom™ processor N450 Single Core/D510 Dual Core 1.66 GHz + ICH8M)

Host development system#

- QNX Momentics 6.5.0, one of the following host systems:
  - QNX Neutrino 6.5.0
  - Windows Vista
  - Windows 7
  - Linux - Ubuntu Workstation 9.04 or newer
- 150 MB of free disk space
- RS-232 serial port
- 64 MB of RAM

What's new?#

startup#

- New processors (ex. core i3, i5, i7) are now correctly identified
- By default startup-apic will now use High Precision Event Timer 0 for the system clock (instead of the 8254) on Intel based platforms.
- For certain Atom based platforms, target would hang when running 'shutdown'
- Startup now set the CR4MSE bit on chips that support it
- Latest IOAPIC related fixes are included

pci-bios-v2#

- Fixed a problem in check_range function that was causing problems with PCI/PCI bridges.
- Changed the code in pci_alloc_irq() to only allocate every second item in the IRQ list when MSI/X interrupts are requested. Also reduced the maximum number of interrupts to 16.
- Added a check in avail_irq for a no-connection instance. (0xff)

devnp-e1000.so

- Updated driver to correctly display SerDes in nicinfo and also fixed a problem with link detection
- Changed init and event logic so that MSIX interrupts call directly into their respective interrupt service routines.
- Fixed a problem where the RCTL bits have changed for later chipsets.
- Made a change to stop the 82583V chipset from using MSI-X. According to Intel, the device doesn't support MSI-X.
- Updated the driver to support the 82579 chipset.